UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,437	10/16/2003	Sang Hoo Dhong	ROC920030114US1	8772

30206 7590 02/01/2007

IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
DO, CHAT C	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/687,437	DHONG ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities:

Re claim 2, it is missing a period or a dot (.) at the end of the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-24 cite a method and apparatus of determining the interval of which the sum of two numbers is resided according to a mathematical algorithm. In order for claims to be statutory, claims must either include a practical application or a concrete, useful, and tangible result. However, claims 1-24 merely disclose steps of determining the interval in hardware without disclosing the practical application or tangible result. Thus, claims 1-24 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 7-8, 11-13, 17-19, and 21-24 are rejected under 35 U.S.C. 103(a) as being obvious over the admitted prior art in view of Taborn et al. (U.S. 5,550,767).

Re claim 1, the admitted prior art discloses in Figure 2 a method of determining in which of n intervals a sum of two or more numbers resides (e.g. page 1 lines 22-31 of the original specification) comprising: determining the two or more numbers (e.g. A and B in Figure 2); and providing compress circuits (e.g. n-bit 3:2 in Figure 2) each adapted to: input the two or more numbers (e.g. A and B operands); input range information regarding ranges used to define the n intervals (e.g. R0-R3); and compress the two or more numbers and the range information into two or more outputs (e.g. cr0-sr3); and employing compress circuits to determine in which of the n intervals the sum of the two or more numbers resides (e.g. output of sign check circuit f0-f3 and page 1 lines 10-31 of original specification). The admitted prior art fails to disclose the fewer than n compress circuit. However, Taborn et al. disclose in Figure 1-4 the similar methods using the fewer than n compress circuit (e.g. there are 3 ranges in Figure 4 wherein there is only one adder 25 in Figure 1). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the fewer than n compress circuit as seen in Taborn et al.'s invention into the admitted prior art's Figure 2 because it would enable to reduce the circuitry (e.g. wherein all the adder n-bit 3:2 are the same as seen in Figure 2).

Re claim 2, the admitted prior art further discloses in Figure 2 the two or more numbers are related to an exponent of a first floating point number and an exponent of a second floating point number (e.g. page 1 lines 17-21 of original specification).

Re claim 3, the admitted prior art further discloses in Figure 2 the two or more numbers are related to an exponent of a floating point addend and an exponent of a floating point product (e.g. page 1 lines 17-21 of original specification).

Re claim 7, the admitted prior art further discloses in Figure 2 employing fewer than n compress circuits to determine in which of the n intervals the sum resides comprises: determining a sign check bit for each interval (e.g. as sign check for all the ranges R0-R3 in Figure 2); and determining in which interval the sum resides based on the sign check bit for one or more of the intervals (e.g. page 1 lines 21-31 of original specification).

Re claim 8, the admitted prior art further discloses in Figure 2 employing fewer than n compress circuits to determine in which of the n intervals the sum resides comprises: generating carry and sum bits based on the two or more numbers and range information (e.g. crx and srx respectively in Figure 2); selectively providing the carry and sum bits to a plurality of sign check circuits (e.g. sign check circuits corresponding for R0-R3); determining a sign check bit for each interval based on the selectively provided bits; and determining in which interval the sum resides based on the sign check bit for one or more of the intervals (e.g. Figure 2 and page 1 of original specification).

Re claim 11, the admitted prior art discloses in Figure 2 an apparatus for use in determining in which of n intervals a sum of two or more numbers resides (e.g. page 1

lines 22-31 of the original specification) comprising: compress circuits each adapted to input the two or more numbers (e.g. A and B operands in Figure 2); input range information regarding ranges used to define the n intervals (e.g. R0-R3 in Figure 2); and compress the two or more numbers and the range information into two or more outputs (e.g. crx and srx respectively); and a plurality of sign check circuits coupled to the compress circuits (e.g. sign check circuits 202x), the sign check circuits adapted to generate a sign check bit that corresponds to each of the n intervals based on the two or more outputs generated by the compress circuits (e.g. Figure 2). The admitted prior art fails to disclose the fewer than n compress circuit. However, Taborn et al. disclose in Figure 1-4 the similar methods using the fewer than n compress circuit (e.g. there are 3 ranges in Figure 4 wherein there is only one adder 25 in Figure 1). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the fewer than n compress circuit as seen in Taborn et al.'s invention into the admitted prior art's Figure 2 because it would enable to reduce the circuitry (e.g. wherein all the adder n-bit 3:2 are the same as seen in Figure 2).

Re claim 12, it has similar limitations cited in claim 2. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 13, it has similar limitations cited in claim 3. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 17, the admitted prior art further discloses in Figure 2 the two or more outputs of each compress circuit comprise a sum vector and a carry vector each having a plurality of bits (e.g. A and B operands).

Re claim 18, the admitted prior art further discloses in Figure 2 a plurality of signal paths adapted to selectively route the bits of the carry and sum vectors of each compress circuit to the plurality of sign check circuits (e.g. Figure 2).

Re claim 19, the admitted prior art further discloses in Figure 2 the sign check circuits are adapted to determine a sign check bit for each interval based on the selectively routed sum and carry bits (e.g. sign check circuits in Figure 2 and page 1 of original specification).

Re claim 21, it has similar limitations cited in claim 8. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 22, it has similar limitations cited in claim 17. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 17.

Re claim 23, the admitted prior art further discloses in Figure 2 the range information comprises a plurality logic 0 bits (e.g. inherently as binary number).

Re claim 24, the admitted prior art further discloses in Figure 2 the range information comprises a plurality of logic 1 bits (e.g. inherently as binary number).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,115,725 to Shibata et al. disclose a semiconductor arithmetic apparatus.

b. U.S. Patent No. 5,027,308 to Sit et al. disclose a circuit for adding/subtracting two floating point operands.

c. U.S. Patent No. 7,043,516 to Wolrich et al. disclose a reduction of add-pipe logic by operand offset shift.

d. U.S. Patent No. 6,205,461 to Mansingh discloses a floating-point arithmetic logic unit leading zero count using fast approximate rounding.

e. U.S. Patent No. 5,166,898 to Ishihara discloses a shift amount floating-point calculating circuit with a small amount of hardware and rapidly operable.

f. U.S. Patent No. 6,826,588 to Bhushan et al. disclose a method and apparatus for a fast comparison in redundant form arithmetic.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

January 29, 2007